

34. (New) The module according to claim 30, wherein the connectors are provided in a computer.

35. (New) The module according to claim 30 wherein the connectors are provided on a printed circuit board.--

REMARKS

By this Amendment, Applicant amends claims 1, 13, and 26 to more appropriately define the invention; and adds new claims 27-35 to protect additional aspects related to the present invention. Claims 1-23 and 25-35 are pending.

In the Office Action ("OA"), the Examiner rejected claims 1 and 12 under 35 U.S.C. § 102(b) as anticipated by Buck, U.S. Patent No. 5,203,721 ("Buck"); rejected claims 2-11, 13-15, 18, 19, and 21-23 under 35 U.S.C. § 103(a) as unpatentable over Buck; rejected claims 1-23 and 26 under 35 U.S.C. § 103(a) as unpatentable over Kumar et al., U.S. Patent No. 4,810,917 ("Kumar") in view of Chen, Ultra-Thin Electronic Device Package, Electronic Components and Technology Conference, 1999 ("Chen"); and objected to claim 25 as being dependent upon a rejected base claim, but indicated that it would be allowable if rewritten in independent form including all the recitations of the base claim and any intervening claims.

Applicant again thanks the Examiner for indicating allowable subject matter. Applicant points out that claim 25 was rewritten in independent form in the Amendment dated September 19, 2002 ("Sept. 19th Amendment"). Thus, Applicant submits that the objection to claim 25 is moot.

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With regard to the rejections, Applicant respectfully traverses these rejections for the following reasons.

I. Response to Rejections under 35 U.S.C. § 102(e)

The Examiner alleged that Buck anticipates claims 1 and 12. In response, Applicant submits that Buck fails to anticipate claims 1 and 12 because Buck does not teach all the claim elements.

In order to properly anticipate Applicant's claimed invention under 35 U.S.C. § 102(b), each and every element of the claim in issue must be found, either expressly described or under principles of inherency, in a single prior art reference. Furthermore, "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." See M.P.E.P. § 2131 (8th Ed., Aug. 2001), *quoting Richardson v. Suzuki Motor Co.*, 868 F.2d 1126, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). Finally, "[t]he elements must be arranged as required by the claim." M.P.E.P. § 2131, p. 2100-69.

Claim 1 is directed to a semiconductor device comprising a combination of elements including, *inter alia*, "a cylindrical substrate having wirings formed thereon; and at least one semiconductor chip mounted on a circumferential surface of said substrate ... wherein a diameter of the cylindrical substrate is smaller than a width of the at least one semiconductor chip" (emphasis added).

Buck is directed to a side tap assembly of a coaxial electric signal cable. Buck illustrates that pins 16 and 17 are arranged on the side surface of the coaxial electric signal cable and that an integrated circuit chip 19 is connected to pins 16 and 17. Buck, Fig. 3. The Examiner alleges that integrated circuit chip 19 corresponds to a

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semiconductor chip mounted on a cylindrical substrate 5. (OA, p. 2). Contrary to the Examiner's allegations, Buck differs from the invention recited in claim 1.

Buck relates to a coaxial electric signal cable, but does not disclose a combination of a cylindrical substrates having wirings and a semiconductor chip, or multilayered semiconductor chips, having bumps. More particularly, Buck only illustrates conductive braid shielding 3 and connection pins 16 and 17. See Buck, Fig. 3. Moreover, the device illustrated in Fig. 3 of Buck comprises a conductive braid shielding 3 and conductive area 18, both of which are electrically connected to pins 17, not bumps. Furthermore, Buck discloses that the diameter of the coaxial electric signal cable is greater than the width of the integrated circuit chip 19. See Buck, Fig. 3 and col. 3, lines 35-37. Therefore, Buck fails to teach or suggest at least "a cylindrical substrate having wirings formed thereon ... wherein a diameter of the cylindrical substrate is smaller than a width of the at least one semiconductor chip," as recited in claim 1 (emphasis added). Thus, Buck fails to anticipate claim 1 because Buck fails to teach all the claim elements. For at least this reason, claim 1 is allowable.

Claim 12 is allowable at least due to its dependence from allowable claim 1.

II. Response to Rejections under 35 U.S.C. § 103(a)

The Examiner alleged that claims 2-11, 13-15, 18, 19, and 21-23 are unpatentable over Buck and that claims 1-23 and 26 are unpatentable over Kumar in view of Chen. In response, Applicant respectfully asserts that a *prima facie* case of obviousness has not been established for these claims. Each rejection will now be addressed separately.

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A. Buck

Applicant submits that a *prima facie* case of obviousness has not been established at least because Buck fails to teach or suggest all the claim elements.

In order to establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim elements. Furthermore, "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art." See M.P.E.P. § 2143.01, quoting *In re Wilson*, 424 F.2d 1382, 1385, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or to combine reference teachings. Third, there must be a reasonable expectation of success. See M.P.E.P. § 2143, pp. 2100-122 to 127.

Claim 13 is directed to a semiconductor device comprising a combination of elements including, *inter alia*, "a cylindrical substrate having wirings formed thereon; and at least one stacked body mounted on a circumferential surface of said substrate, said stacked body including a plurality of semiconductor chips stacked one upon the other ... a diameter of the cylindrical substrate is smaller than a width of each of the semiconductor chips" (emphasis added). As advanced above for claim 1, Buck fails to teach or suggest at least this claim element. Thus, a *prima facie* case of obviousness has not been established for claim 13. For at least this reason, claim 13 is allowable.

Claims 2-11 are allowable at least due to their dependence from allowable claim

1. Claims 14, 15, 18, 19, and 21-23 are allowable at least due to their dependence from allowable claim 13. "If an independent claim is nonobvious under 35 U.S.C. 103, then

any claim depending therefrom is nonobvious." M.P.E.P. § 2143.03, p. 2100-126 citing *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988).

Additionally, the Examiner alleged that stack chips were well-known to one skilled in the art at the time of the invention. Further, the Examiner alleged that "[b]ecause applicant did not traverse the merits of the official notice statement, it has been deemed that applicant acknowledged the well-known technology and has waived its right to later object." (OA, p. 6). M.P.E.P § 2144.03 sets forth the time period for challenging an Examiner's official notice statement. The M.P.E.P. recites "[a] seasonable challenge constitutes a demand for evidence made as soon as practicable during prosecution. Thus, Applicant is charged with rebutting the well known statement in the next reply after the Office action in which the well known statement was made." M.P.E.P § 2144.03, pp. 2100-129 to 130.

Applicant did not request that the Examiner provide a reference in support of the Official Notice allegation made in the June 16, 2002 Office Action ("June 16th OA") because there was insufficient legal basis for the Examiner to have taken Official Notice in the first place. By traversing the improper 35 U.S.C. § 102 rejection, Applicant was, in fact, traversing the lack of a legal basis for even postulating an Official Notice-based rejection, and that by challenging, in this response, the new "Office Notice" Applicant will have seasonably challenged such Notice. Applicant bases this assertion on two points: 1) the improper nature of the original rejection, and 2) policy behind the seasonal traversal.

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1) Improper Nature of The Original Rejection

In the June 16th OA, the Examiner admitted that "Buck does not appear to disclose a plurality of chips stacked one upon the other to form a stacked body on a surface of said substrate, or a plurality of stacked bodies arranged at predetermined distance apart in the outer circumferential direction of said substrate," and that "Buck does not appear to show a chip sealed with a resin." (Office Action, p.3, ¶ 10-12, emphasis added). The Examiner, in this rejection, took "Official Notice" that certain features are "obvious to one of ordinary skill in the art." (June 16th OA, p.3, ¶ 10-12, emphasis added).

In response to this rejection, Applicant traversed this rejection as being improper. More particularly, Applicant pointed out that for anticipation under 35 U.S.C. § 102(b), each and every element of the claim in issue must be found, either expressly described or under principles of inherency, in a single prior art reference. See M.P.E.P. § 2131, pp. 2100-68 to 69. In fact, the Examiner admitted that Buck fails to disclose several claim recitations. Furthermore, Applicants pointed out that rationale based on common knowledge in the art or "well-known" prior art (i.e. "Official Notice"), while available to support a obviousness-type rejection (in certain cases), is not appropriate in an anticipation rejection. M.P.E.P. § 2144.03, pp. 2100-129 to 130. In other words, the Examiner, in an anticipation rejection under 35 U.S.C. § 102, cannot argue legal obviousness, including reliance on common knowledge. As stated above, the Examiner, in making an anticipation rejection, took "Official Notice" that certain features are "obvious to one of ordinary skill in the art." (June 16th OA, p.3, ¶ 10-12, emphasis added). Clearly, this was not a proper ground of rejection. Accordingly, a proper

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traversal of this "Official Notice" would have been to point out that "Official Notice" as applied by the Examiner is not applicable to an anticipation rejection, which Applicant expressly did. (Sept. 19th Amendment, pp. 9-10).

Moreover, in the present Office Action, the Examiner rejected the claims under 35 U.S.C. § 103(a) as unpatentable over Buck and takes "Official Notice" regarding certain claim elements. This rejection is a new rejection, and the "Official Notice" taken in support of this rejection is being presented for the first time. Applicant has had no opportunity except in this response to traverse the "Official Notice" taken in this new rejection under 35 U.S.C. § 103(a). Thus, Applicant submits that a traversal in this response is seasonal because the traversal is being presented in the first response after presentation of the "Official Notice" having an appropriate legal basis.

2) Policy Behind Seasonal Traversal

The policy behind the requirement of a seasonal traversal of Office Notice is to prevent undue burden on the Examiner and allow the Examiner a chance to respond to Applicant's traversal. Specifically, a seasonal traversal "is necessary because the examiner must be given the opportunity to provide evidence in the next Office action or explain why no evidence is required". M.P.E.P § 2144.03, pp. 2100-129 to 130. Thus, for example, it would not be seasonable to traverse an Official Notice on appeal because the Examiner would not have a chance to present evidence or arguments. See *In re Chevenard*, 139 F.2d 711, 713 (C.C.P.A. 1943).

In the present case, there is no undue burden placed on the Examiner. Since the present Office Action is non-final, prosecution of the merits is still open. Thus, the Examiner has ample opportunity to respond to Applicant's traversal.

Accordingly, Applicant expressly and seasonably traverses the Examiners taking "Official Notice" that it is well-known to stack chips as recited in the claims. The Examiner is respectfully reminded of the provisions of M.P.E.P. § 2144.03, the procedures set forth in the Memorandum by Stephen G. Kunin, Deputy Commissioner for Patent Examination Policy dated February 21, 2002, and the precedents provided in *Dickinson v. Zurko*, 527 U.S. 150, 50 U.S.P.Q.2d 1930 (1999) and *In re Ahlert*, 424 F.2d, 1088, 1091, 165 U.S.P.Q. 418, 420 (CCPA 1970). An "Official Notice" rejection is improper unless the facts asserted are well-known or common knowledge in the art, and capable of instant and unquestionable demonstration as being well-known. Further, any facts asserted as well-known should serve only to "fill in the gaps" in an insubstantial manner. It is never appropriate to rely solely on "common knowledge" without evidentiary support in the record as the principal evidence upon which a rejection is based.

Applicant submits that chip stacking, as set forth in the claims, is not unquestionably well-known, and the Examiner has failed to demonstrate such. Further, considering the assertions on the record, it appears the Examiner is attempting to improperly rely on "Official Notice" as the basis upon which to justify the rejection. Accordingly, Applicant traverses the "Official Notice" and requests that the Examiner withdraw the rejection and timely allow the pending claims. However, if the Examiner maintains his position that the pending claims are not allowable, Applicant requests that the Examiner cite a competent prior art reference in substantiation of these unsupported conclusions and set forth a proper rejection based on factual evidentiary support that is made of record.

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Also, the Examiner admitted that Buck fails to teach or suggest a plurality of chips on the inner surface and stacked bodies. (OA, p. 3). The Examiner alleged that it would be obvious to duplicate chips since it has been held "that mere duplication of essential working parts of a device involves only routine skill in the art." (OA, p. 3). The Examiner cited *St. Regis Paper Co. v. Bemis Co.*, 193 U.S.P.Q. 8 (Ca App. 7th 1977) and *In re Harza*, 124, U.S.P.Q. 378 (C.C.P.A. 1960). Applicant submits that the Examiner has misapplied these two cases because the facts of the two cases are not similar to the subject application.

In a rejection, the Examiner may use the rationale of legal precedent established by prior case law, subject to the following considerations. "The examiner must apply the law consistently to each application after considering all the relevant facts. If the facts in a prior legal decision are sufficiently similar to those in an application under examination, the examiner may use the rationale used by the court." M.P.E.P. § 2144, pp. 2100-127 (emphasis added).

In *In re Harza*, the claims under appeal regarded a web sealing in masonry materials. *In re Harza*, 124 U.S.P.Q. at 379. The claimed web comprised ridges on each side of the web. *Id.* at 360. The prior art Gardner applied by the Examiner taught a web with a single ridge on each side of the web. *Id.* The court held that mere duplication of the ridges does not have patentable significance. *Id.* In *St. Regis Paper Co. v. Bemis Co.*, the court similarly held duplication of part is obvious in relation to the use of multiple layers in a bag. *St. Regis Paper Co. v. Bemis Co.*, 193 U.S.P.Q. at 11.

The present claims recite a plurality of semiconductor chips (e.g. claim 2). Unlike *In re Harza* and *St. Regis Paper Co. v. Bemis Co.*, the addition of multiple chips is not

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mere duplication. More particularly, each chip of the plurality of chips may have a different function and structure. The prior art, Buck, illustrates only one chip. See Buck, Fig. 3. Thus, one skilled in the art could not duplicate Buck's chip in order to teach the multiple chips of the present claims because claimed plurality of chips may have different functions and structures. Thus, Applicant submits that the reasoning of *In re Harza* and *St. Regis Paper Co. v. Bemis Co.* is not applicable.

B. Kumar in view of Chen

The Examiner alleged that claims 1-23 and 26 are unpatentable over Kumar in view of Chen. Applicant submits that a *prima facie* case of obviousness has not been established because Kumar and Chen, taken alone or in combination, fail to teach or suggest all the elements of the claims.

Claim 1 recites, *inter alia*, "a cylindrical substrate having wirings formed thereon; and at least one semiconductor chip mounted on a circumferential surface of said substrate ... wherein a diameter of the cylindrical substrate is smaller than a width of the at least one semiconductor chip" (emphasis added). Claim 13 recites, *inter alia*, "a cylindrical substrate having wirings formed thereon; and at least one stacked body mounted on a circumferential surface of said substrate, said stacked body including a plurality of semiconductor chips stacked one upon the other ... a diameter of the cylindrical substrate is smaller than a width of each of the semiconductor chips" (emphasis added).

Claim 26 is directed to a method of manufacturing a semiconductor device comprising a combination of elements including, *inter alia*, "mounting at least one semiconductor chip having bumps on at least a region of a surface of a flexible substrate; and bending said substrate into a cylindrical form, wherein a diameter of the

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cylindrical substrate is smaller than a width of the at least one semiconductor chip"

(emphasis added).

Kumar is directed to a digital resolver/encoder device. Kumar discloses that the digital resolver/encoder device is applied to a motor. Kumar discloses that a circuit device such as a PROM is disposed on a flexible circuit board 18. See Kumar, Figs. 3 and 4. Furthermore, Kumar discloses that flexible circuit board 18 is rolled or coiled into a generally cylindrical shape 20. Kumar, col. 3, lines 41-50. However, Kumar the circuit device, e.g., the PROM, is not a semiconductor chip itself; but is a device housed in a package. Moreover, Kumar discloses that the diameter of the cylindrical-shaped flexible circuit board 18 is set to be greater than the size of the circuit device. See Kumar, Figs. 2 and 4. Thus, Kumar fails to disclose a cylindrical substrate having a diameter smaller than the width of a semiconductor chip.

Moreover, Chen discloses a ultra-thin electric device package. Chen discloses that a thin chip is mounted on a flex circuit. See Chen, Figs. 2 and 3. Chen discloses that the flex circuit is wrapped around a soft drink can, and the flex circuit is twisted. See Chen, Fig. 2. Namely, Chen discloses a structure in which a flexible package on which a semiconductor chip is mounted is slightly curved or twisted. However, Chen does not disclose or even suggest a cylindrical substrate having a smaller diameter than the width of the semiconductor chip. Thus, Chen fails to disclose a cylindrical substrate having a diameter smaller than the width of a semiconductor chip.

Therefore, Kumar and Chen, taken alone or in combination, fail to teach or suggest all the elements of claims 1, 13, and 26. Hence, a *prima facie* case of

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obviousness has not been established. For at least this reason, claims 1, 13, and 26 are allowable.

Claims 2-11 are allowable at least due to their dependence from allowable claim

1. Claims 14-23 are allowable at least due to their dependence from allowable claim

13. M.P.E.P. § 2143.03, p. 2100-126.

Furthermore, Applicant traverses the Examiner taking "Official Notice" that it is well known to form bumps on chips as recited in the claims. Applicant submits that bumps, as set forth in the claims, is not unquestionably well-known, and the Examiner has failed to demonstrate such. Further, considering the assertions on the record, it appears the Examiner is attempting to improperly rely on "Official Notice" as the basis upon which to justify the rejection. Accordingly, Applicant expressly traverses the "Official Notice" and requests that the Examiner withdraw the rejection and timely allow the pending claims. However, if the Examiner maintains his position that the pending claims are not allowable, Applicant requests that the Examiner cite a competent prior art reference in substantiation of these unsupported conclusions and set forth a proper rejection based on factual evidentiary support that is made of record.

III. New Claims

Applicant adds new claims 27-35 to protect additional aspects related to the present invention. Claims 27, 28, and 29 depend from claims 1, 13, and 26, respectively. For at least the reason advanced above, claims 27, 28, and 29 are patentable at least due to their dependences from allowable claims 1, 13, and 26.

Furthermore, claim 30 is directed to a semiconductor module comprising a combination of elements including, *inter alia*, "a cylindrical substrate having wirings formed thereon; at least one semiconductor chip mounted on a circumferential surface

of said substrate, said semiconductor chip being bent along the surface of said substrate and having bumps in contact with the wirings; and a plurality of terminals to be connected to connectors, the terminals being formed on the cylindrical substrate and connected to the wirings." As advanced above, the inventions disclosed in Buck, Kumar, and Chen neither disclose nor suggest at least a cylindrical substrate with at least one semiconductor chip mounted thereon as recited in claim 30. Thus, claim 30 is patentable over Buck, Kumar, and Chen. Claims 31-35 are patentable at least due to their dependence from patentable claim 30.

IV. Conclusion

In view of the foregoing, Applicant respectfully requests the reconsideration and reexamination of this application and the timely allowance of the pending claims.

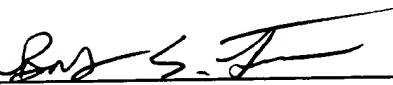
Attached hereto is a marked-up version of the changes made to the claims by this Amendment. The attachment is captioned "**Appendix to Amendment of April 3, 2003**".

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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Dated: April 3, 2003

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Appendix to Amendment of April 3, 2003

IN THE CLAIMS:

Please amend claims 1, 13, and 26, and add new claims 27-35, as follows:

1. (Twice Amended) A semiconductor device, comprising:

a cylindrical substrate having wirings formed thereon; and

at least one semiconductor chip mounted on a circumferential surface of said substrate, said semiconductor chip being bent along the surface of said substrate and having bumps in contact with the wirings,

wherein a diameter of the cylindrical substrate is smaller than a width of the at least one semiconductor chip.

13. (Twice Amended) A semiconductor device, comprising:

a cylindrical substrate having wirings formed thereon; and

at least one stacked body mounted on a circumferential surface of said substrate, said stacked body including a plurality of semiconductor chips stacked one upon the other and being bent along the surface of said substrate, wherein each of said semiconductor chips has bumps, [and] the bumps formed on one of said semiconductor chips are connected to said wirings, and a diameter of the cylindrical substrate is smaller than a width of each of the semiconductor chips.

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26. (Twice Amended) A method of manufacturing a semiconductor device, comprising:

mounting at least one semiconductor chip having bumps on at least a region of a surface of a flexible substrate; and

bending said substrate into a cylindrical form,

wherein a diameter of the cylindrical substrate is smaller than a width of the at least one semiconductor chip.